HILL

Our Client is an international company operating in the field of chip verification. For start-up of their business operations in Serbia, with office in Novi Sad, they are currently looking for a

Verification Engineer for Functional Verification

- Novi Sad -

Responsibilities:

- RTL coding using VHDL or Verilog
- test bench generation using Verilog, SystemVerilog or SystemC and ideally eLanguage
- development of Verification Plan and associated testcases
- setup of simulation environment for regression
- gate-level simulation

Requirements:

- university degree in electronics, electrotechnics, information technology or equivalent
- several years of experience in digital design and debug based on VHDL and/or Verilog HDL in a UNIX workstation environment
- good knowledge of Verification methodologies and tools (Cadence, Mentor)
- excellent communication and interpersonal skills
- fluency in English and readiness to travel are prerequisites

Our Client offers you an excellent opportunity for further career advancement within highly stimulating international environment, together with competitive working conditions.

If you recognized yourself in the above description and would like to become a part of our Client's start up team in Serbia, please send your CV and application letter in English to our address, with full confidentiality.

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